**P-N JUNCTION DIODE**

**AIM:**
To study V-I Characteristics of P-N Junction diode in forward biased condition.

**APPARATUS REQUIRED:**
Multimeter, diode, Resistance, Bread board, DC power Supply, connecting wires.

**CIRCUIT DIAGRAM:**

**THEORY:**
The graph plotted between the potential difference across the PN Junction and the circuit current is known as V-I Characteristics of a P-N Junction or a diode. With forward bias to the P-N Junction very little current flows until the forward voltage exceeds the junction barrier potential (0.3v for Ge and 0.7 for Si). As the forward voltage reaches beyond the knee of the characteristics, the potential barrier is completely eliminated, forward current increases almost linearly. If the forward voltage is increased, extremely large current will flow and the diode may get destroyed due to over heating.

**OBSERVATION:**
<table>
<thead>
<tr>
<th>S.NO.</th>
<th>Voltage (V)</th>
<th>Current (I)</th>
</tr>
</thead>
</table>

**PRECAUTIONS:**

1. Connections should be tight and easy to inspect.
2. Handle the power supply and multimeters carefully.
3. Observations should be taken carefully.

**RESULT**
ZENER DIODE.

AIM:

To Study the V-I Characteristics of Zener Diode.

APPARATUS REQUIRED:

Multimeter, Breadboard, resistance, Zener Diode, D.C Voltage Supply etc.

CIRCUIT DIAGRAM:

![Circuit Diagram](image)

THEORY

The zener diode, also sometimes called the (Breakdown diode) is a PN Junction diode specially designed for operation in the breakdown region in reverse bias condition. When an ordinary PN junction diode is reverse biased normally only very small reverse saturation current flows. This current is due to movement of minority carriers. However, if the reverse biased is increased, a point is reached when the function breaks down and the reverse current increases abruptly, as shown in figure. The critical value of the voltage, at which the breakdown of a PN Junction diode occurs is called the breakdown voltage.

Observation:
(1). Connections should be tight and easy to inspect.

(2). Handle the power supply and multimeters carefully.

(3). Observations should be taken carefully.

RESULT:
To study input and output characteristic of transistor in case of Common Emitter Configuration.

**APPARATUS REQUIRED:**

Transistor Kit, Connecting Wires, 3 millimeters.

**THEORY**

**Input characteristic:-**

The curve drawn b/w the base current IB and base emitter voltage VCE for a given value of collector emitter voltage VCE is known as input characteristic. The current is small as long as VBE is less than the barrier voltage. When VBE is greater voltage, the curves similar to that of a forward biased diode. More than 95% emitter electrons and emitter holes go to the collector to form the collector current. That is why IB is much smaller (in microampere).
**Output Characteristics:**

It is the curve drawn b/w collector current IC and collector emitter voltage VCE for a given value of base current IB.

1. The collector current IC varies with VCE for VCE between 0 to 1v than become greater than become almost constant and independent of VCE. The transistors are always operating above.

2. Output characteristics of CE configuration has same slope while CB configuration has almost horizontal configuration.

3. In active region, for small values of base current IB the effect of collector voltage VC, over IC is small but for large values of IB this effect increases.

4. In cut-off region, small amount of collector current IC flows even when base current IB=0. This is called ICB moderates o/p to i/p impedance ratio makes this configuration an ideal one for coupling between various transistor stages. Output characteristics are used to find DC current gain BO.

\[ B = \frac{IC}{IB} \quad B_0 = \frac{IC}{IB} \quad VCE = \text{Constant} \]

**Observation:**

<table>
<thead>
<tr>
<th>Input Characteristics S. No.</th>
<th>VCE = 0V</th>
<th>VCE = 2V</th>
<th>VCE = 6V</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBE IB</td>
<td>VBE IB</td>
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</table>
## Output Characteristics

<table>
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<tr>
<th>S. No.</th>
<th>IB = 0</th>
<th>IB=20μA</th>
<th>IB= 80μA</th>
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<tbody>
<tr>
<td></td>
<td>IC</td>
<td>VCE</td>
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**PRECAUTIONS:**

(1). Connections should be tight and easy to inspect.

(2). Handle the power supply and multimeters carefully.

(3). Observations should be taken carefully.

**RESULT:**
AIM:

To Measure Frequency Response of an R-C Coupled Amplifier

APPARATUS REQUIRED:

R-C coupled amplifier Kit, CR0, function generator, CR0 probes

CIRCUIT DIAGRAM:

A cascaded arrangement of CE transistor stages is shown. The output $Y_1$ of one stage is coupled to the input $X_2$ of the next stage via a blocking capacitor $C_b$ which is used to keep the dc component of the output voltage at $Y_1$ from reaching the input $X_2$. $R_g$ is from gate to ground, and the collector circuit resistor is $R_e$ ($R_d$). The source resistor $R_s$, the emitter resistor $R_e$ and the resistances $R_i$ and $R_2$ are used to establish the bias. The bypass capacitors used to prevent loss of amplification due to -ve feedback, are $C_2$ in the emitter circuit and $C_s$ in the source circuit. Also present junction capacitances to be taken into account when we consider the high frequency response, which is limited by their presence. We assume that the active device operates linearly so that small signal modes are used.

THEORY:
Most amplifiers have relatively constant gain across a range, or band, of frequencies. This band of frequencies is referred to as the bandwidth of the circuit. A frequency-response curve is a graphical representation of the relationship between amplifier gain and operating frequency. A generic frequency response curve is shown in Figure. This particular curve illustrates the relationship between power gain and frequency. As shown:

The circuit power gain remains relatively constant across the mid band range of frequencies. As operating frequency decreases from the mid band area of the curve, a point is reached where the power gain begins to drop off. The frequency at which power gain equals 50% of its midband value is called the lower cutoff frequency (fc1). As operating frequency increases from the midband area of the curve, a point is reached where the power gain begins to drop off again. The frequency at which power gain equals 50% of its midband value is called the upper cutoff frequency (fc2).

Note that the bandwidth of the circuit is found as the difference between the cutoff frequencies. By formula,

\[ BW = f_{c2} - f_{c1} \]

The geometric center frequency (\(\omega_0\)) of an amplifier is the geometric average of the cutoff frequencies, found as
\[ f_0 = \sqrt{f_{c1} f_{c2}} \]

Power gain is maximum when an amplifier is operated at its geometric center frequency. As frequency varies above (or below) the power gain decreases slightly. By the time one (or the other) cutoff frequency is reached, power gain has dropped to half its midband value.

The relationship between \( f_0, f_{c1} \) and \( f_{c2} \) also be described using frequency ratios, as follows:

\[ \frac{f_0}{f_{c1}} = \frac{f_{c2}}{f_0} \]

The relationship allows us to calculate the value of either cutoff frequency when the values of the geometric center frequency and the second cutoff frequency are known. The relationships used are

\[ f_{c1} = \frac{f_0^2}{f_{c2}} \]
\[ f_{c2} = \frac{f_0^2}{f_{c1}} \]

**Measuring the Cutoff Frequencies:**

The cutoff frequencies of an amplifier can be measured with an oscilloscope using the following procedure:

1. Set up the amplifier for the maximum undistorted output signal.
2. Establish that you are operating in the midband frequency range by varying the frequency of the input signal several kilohertz in both directions. If you are in the midband range, slight variations in operating frequency will not cause any significant changes in the output amplitude of the circuit.
3. If you are not at midband, adjust \( f_{c1} \) until you are.
4. Adjust the volts/division calibration control on the oscilloscope until the amplifier output waveform fills exactly seven major divisions (peak-to-peak).

5. To measure the value of $f_{c1}$ decrease the operating frequency until the amplifier output waveform fills only five major divisions. At this frequency, the amplitude of the amplifier has dropped to $5\pi 0.707$ its maximum value. This indicates that we are operating at the lower cutoff frequency.

6. To measure the value of $f_{c2}$, increase the operating frequency until the same thing happens on the high-frequency end. The frequency at which this occurs is $f_{c2}$.

Be sure to use the x10 probe to minimize the effect of the oscilloscope input capacitance on the frequency measurements.

The value of 0.707 is based on the relationship between voltage and power. Power changes with the square of voltage. When voltage gain drops to $0.707Ar(mid)$ power gain drops by a factor of $(0.707)^2 = 0.5$ (which is half its midband value).

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<thead>
<tr>
<th>S.No.</th>
<th>Frequency(Hz)</th>
<th>Output voltage( V)</th>
<th>Voltage gain</th>
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**OBSERVATION:**

**RESULT:**
INVERTING & NON INVERTING AMPLIFIER USING OP AMP

AIM:

Design and Realize Inverting & Non inverting Amplifier using Op amp.-

APPARATUS REQUIRED:

Op-amp (741) CRO, connecting wires function generator and CRO probes.

CIRCUIT DIAGRAM:
**THEORY:**

Op-amp is an amplifier having very high frequency, high voltage gain, infinite input impedance and zero output impedance the ideal op-amp represent a perfect voltage amplifier and is often referred as voltage controlled voltage source. LM741IC has voltage gain of 10000, a unity gain, frequency of 1Mhz and input impedance of 2 Mega ohm.

**Inverting Amplifier** :- It is the most basic of op-amp it use feedback to stabilize overall voltage gain. At inverting terminal input Vin is applied through R1. This result in an inverting output Vo.

The input voltage to produce an inverted output, the output voltage feedback to input through R2. This result in negative feedback because output is 180 out of phase with input.

**Non-inverting Amplifier** :- The basic of non inverting amplifier is given in fig. The output voltage is feedback to input through voltage divider. The voltage across R1 is feedback voltage applied at inverting terminal this feedback voltage almost equal to input voltage.

**Voltage Gain** :- Due to virtual short, Input voltage across R1 is

\[ \text{Vin} = I1 \times R1 \]

Since no current can flow through a virtual short, same current flow through R1 which means that output voltage is given by

\[ \text{Vo} = - \left( \frac{R2}{R1} \right) \times \text{Vin} \]

Gain, \( \frac{\text{Vo}}{\text{Vin}} = - \frac{R2}{R1} \)

**Voltage Gain** :- Due to virtual short, Input voltage across R1 is

\[ \text{Vin} = I1 \times R1 \]

Since no current can flow through a virtual short, same current flow through R1 which means that output voltage is given by

\[ \text{Vo} = (1+ \frac{R2}{R1}) \times \text{Vin} \]

Gain, \( \frac{\text{Vo}}{\text{Vin}} = 1+\frac{R2}{R1} \)

**OBSERVATION:**

- Connect the circuits as shown in the figure.
- Give power supply through function generator.
- Take input and output waveform from CRO for inverting, non-inverting and buffer amplifier.
- Calculate gain theoretically as well as practically.

**RESULT:**
AIM:
To study an Op-amp as an Adder & a Subtractor using Op-amp

APPARATUS REQUIRED:
Kit containing adder circuit, DC Power (0-10V) and Multimeter

CIRCUIT DIAGRAM:

OP-amp as Adder

Op-amp as Subtractor
1) **ADDER**

The circuit that performs the addition of signals with applications is as shown in fig. using the superposition theorem. This circuit can be used to add ac or dc signals. This circuit provides an output voltage proportional to or equal to the sum of two or more input voltages each multiplied by the constant gain factor. The output voltage can be given in terms of input as:

\[
V_{out} = - R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)
\]

If \( R_1 = R_2 = R_3 = R_f \)
then \( V_{out} = -(V_1 + V_2 + V_3) \)

Hence the circuit act as adder, It adds input voltages.

2) **SUBTRACTOR**

Since differential amplifier amplifies the difference of two input signals applied to the inverting and non inverting terminal of an op-amp., it can be used as subtractor circuit. The circuit is shown in fig. The circuit provides all output equal to the difference of two input signals.

\[
V_{out} = \frac{R_3}{(R_3+R_4)} \times (R_f + \frac{R_1}{R_1})V_1 - (\frac{R_f}{R_1})V_2
\]

If \( R_3 = R_4 \) & \( R_f = R_1 \)
Then \( V_{out} = \frac{R_3}{(2R_3)} \times (2\frac{R_1}{R_1})V_1 - (\frac{R_1}{R_1})V_2 \)
\( V_{out} = V_1 - V_2 \)

**OBSERVATION:**

For Adder
<table>
<thead>
<tr>
<th>S. No.</th>
<th>V1(V)</th>
<th>V2(V)</th>
<th>( V_0 = -(V_1+V_2) ) (Observed)</th>
<th>( V_0 = -(V_1+V_2) ) (Calculated)</th>
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For Subtractor

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<tr>
<th>S. No.</th>
<th>V1(V)</th>
<th>V2(V)</th>
<th>( V_0 ) (v)</th>
<th>( V_0 = (V_1-V_2) ) (Calculated)</th>
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**RESULT:**
To Verify the Operation of a Differentiator Using 741 Op-amp

**APPARATUS REQUIRED:**

CRO, Function generator, Integrator trainer kit, Connecting probes, Trace paper.

**THEORY:**

Its function is to provide an output voltage proportional to the rate of change of the input voltage. It is an inverse mathematical operation to that of an integrator. Differentiator circuit can be obtained by interchanging the resistor and capacitor of the integrator circuit, as shown in fig.

Let \( i \) be the rate of change of charge i.e \( \frac{dq}{dt} \).

Now charge, \( q = C \cdot V_c \)

- So \( i = \frac{dq}{dt} = \frac{d}{dt}(C \cdot V_c) \)
Taking inverting input terminal as virtual ground

Output voltage \( V_0 = -iR = (C \frac{dV_c}{dt})R \)

\[ \text{CR} \frac{dV_c}{dt} \]

i.e. output voltage is proportional to the derivative of the input voltage, the constant of proportionality being \(-CR\). One common application of the op-amp differentiator is to produce very narrow spikes, as shown in fig. The advantage of an opamp differentiator over a simple R-C differentiator is that the spikes produced come from a low-impedance source, which makes driving typical load resistance easier. A differentiator is rarely used in analog computers as it tends to amplify (the output voltage magnitude being proportional to the frequency of the input signal) noise drift and other unwanted disturbance in the system.

**RESULT**
To Verify the Operation of an Integrator Using 741 Op-amp

**APPARATUS REQUIRED:**
CRO, Function generator, Integrator trainer kit, Connecting probes,

**CIRCUIT DIAGRAM:**

**THEORY:**
Integrator is a linear op-amp device. It is made by using a capacitor in feedback circuit of the op-amp instead of a feedback resistance. In this way, the capacitor will store the feedback voltage and during discharge time, the R-C circuit will give a ramp voltage as output. As shown in the circuit diagram,

\[ i_1 = i_2 \]

Here \( i_1 = \frac{V_{in}}{R} \)

And \( V_{out} = -\frac{1}{C} \int i_2 \, dt \)
So \[ V_{out} = -\frac{1}{RC} \int V_{in} \, dt \]

Thus the output voltage is the integration of the input voltage applied at the inverting terminals. If we apply square wave as input, output is triangular wave.

**Integrator As Low Pass Filter:**

Referred to input and output waveform, we observe that input to integrator is a square pulse. The output is in the form of triangular wave. This can be explained by taking R-C circuit, as capacitor charges with constant voltage which varies linearly with time due to constant current \( I_c = I_{in} \) which is due to virtual ground condition. Therefore, ramp signal is generated as capacitor charges and discharges which is the integral part of the input signal. Now, as we know output is taken across capacitor C, which blocks low frequency range and passes high frequency. Therefore, we get output in low frequency range. So integrator acts as low pass filter.

**OBSERVATION:**

Trace the I/p and O/p waveform

**RESULT**
BASIC GATES (AND, OR, NOT)

AIM:
To study basic gates (AND, OR, NOT) and verify their truth tables.

APPARATUS REQUIRED:
LED, IC’s, Wires, 5 volt DC supply, Bread Board etc

THEORY:
AND Gate

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Output Q</th>
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</thead>
<tbody>
<tr>
<td>0</td>
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Traditional symbol                      Truth Table

In AND gate circuit it has n input and only one output. Digital signals are applied in input terminal. In the AND gate operation is ‘t’ if and only if all the input are ‘1’ otherwise zero.

Mathematically

The output Q is true if input A AND input B are both true: \( Q = A \text{ AND } B \)
An AND gate can have two or more inputs, its output is true if all inputs are true.
**OR Gate**

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Output Q</th>
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</table>

Traditional symbol | Truth Table

In OR-Gate operation it has also n input and only one output. In OR operation output is one if and only if one or more input are ‘1’.

Mathematically

The output Q is true if input A OR input B is true (or both of them are true): \( Q = A \ OR \ B \)

An OR gate can have two or more inputs, its output is true if at least one input is true.

**NOT Gate (Inverter)**

<table>
<thead>
<tr>
<th>Input A</th>
<th>Output Q</th>
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<tbody>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
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</table>

Traditional symbol | Truth Table

It is also known as inverter. It has only one input and one output.

Mathematically
The output Q is true when the input A is NOT true, the output is the inverse of the input:
\[ Q = \text{NOT} \ A \]
A NOT gate can only have one input. A NOT gate is also called an inverter.

**PROCEDURE:**

The AND – Gate & OR-Gate operation are same but only difference is their Ic’s number. In AND-Gate 7408 no. Ic’s is used 4 in OR-Gate 7432 no. Ic’s used. In both cases pin no. 7 is ground & pin number 14 is supply or pin 7 is connected to ground and pin 14 is connected to supply 4 ‘1’ and ‘2’ are input and output. Some further 4 & 5 are input and 6 is output. The procedure of NOT – Gate is same as AND & OR operation. The only difference is that in NOT-Gate one pin is input and one is output. The ground and supply pin no. are same as that of AND & OR Gate. In NOT GATE 1 is input and 2 is output like this 3 is input and 4 is output.

**PRECAUTIONS:**

1) Supply should not exceed 5v.
2) Connections should be tight and easy to inspect.
3) Use L.E.D. with proper sign convention and check it before connecting in circuit.

**RESULT**
REALIZATION OF BASIC GATES USING UNIVERSAL GATES

AIM:
To realize Basic gates (AND, OR, NOT gate) using Universal gates (NAND & NOR).

APPARATUS REQUIRED:
LED, IC’s, Wires, 5 volt DC supply, Bread Board etc.

THEORY:

AND Gates to AND, OR, NOT Gates:

AND gates is Universal gate. The Basic gates AND, OR, NOT can be realized from it. The Boolean equations and logic diagrams are as follows:

NAND TO AND:

\[ y = AB \]

NAND TO NOT:

\[ y' = A \]
NAND TO OR :-

\[ y = A + B \]

NOR Gate to AND, OR, NOT Gates:

NOR gate is also an Universal gate. The Basic gates AND, OR, NOT can be realized from it. The Boolean equations and logical diagrams are as follows:

NOR to OR Gate:

\[ y = A + B \]

NOR to AND Gate:

\[ y = AB \]

NOR to NOT Gate:

\[ y \]
Truth tables:

NAND to AND Gate

<table>
<thead>
<tr>
<th>Inputs</th>
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<th>Output</th>
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<tbody>
<tr>
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<td>Y</td>
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NAND to OR Gate

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NAND to NOT Gate

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### NOR to AND Gate

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### NOR to OR Gate

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<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>A</td>
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<tr>
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### NOR to NOT Gate

<table>
<thead>
<tr>
<th>input</th>
<th>output</th>
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<tbody>
<tr>
<td>A</td>
<td>Y</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
1) Supply should not exceed 5v.
2) Connections should be tight and easy to inspect.
3) Use L.E.D. with proper sign convention and check it before connecting in circuit.
AIM:

To study the S-R flip flop & realize its logic circuit & verify its truth table.

APPARATUS REQUIRED:

Bread-board, IC’s no-7400, i.e for NAND gate, wires ,two L.E.D’s, 5V dc supply etc.

CIRCUIT DIAGRAM:

![Circuit Diagram](image1)

THEORY:

Flip flop is generally 1 bit memory cell whose output can be interacted with two inputs ‘S’ and ‘R’. This consists of four NAND gates is ‘S’ & ‘R’ respectively and followed NAND gates are provided with output of these two and outputs from each one to another as shown in fig.

Truth Table:
When $S=1$ and $R=0$

FF is in set conditions i.e $[Q=1, Q'=0]$

And when $S=0$ and $R=1$

FF is in reset condition i.e $[Q=0, Q'=1]$

When $S=R=0$ the output will not change i.e they will remain in last output position. But when $S=R=1$ then both $Q$ & $Q'$ try to be in higher energy state which is not possible hence for S-R flip flop this conditions is not define.

### PRECAUTIONS:

1. Supply should not exceed 5v.
2. Connections should be tight and easy to inspect.
3. Use L.E.D. with proper sign convention and check it before connecting in circuit.
AIM:
To study the J-K Flip –Flop.

APPARATUS REQUIRED:
Connecting wire, 7476 IC, LED, 5v supply etc.

CIRCUIT DIAGRAM:
This is a modified version of an S-R flip-flop with no "invalid" or "illegal" output state. Look closely at the following diagram to see how this is accomplished:

What used to be the S and R inputs are now called the J and K inputs, respectively. The old two-input AND gates have been replaced with 3-input AND gates, and the third input of each gate receives feedback from the Q and not-Q outputs. What this does for us is permit the J input to have effect only when the circuit is reset, and permit the K input to have effect only when the circuit is set. In other words, the two inputs are interlocked, to use a relay logic term, so that they cannot both be activated simultaneously. If the circuit is "set," the J input is inhibited by the 0 status of not-Q through the lower AND gate; if the circuit is "reset," the K input is inhibited by the 0 status of Q through the upper AND gate.

When both J and K inputs are 1, however, something unique happens. Because of the selective inhibiting action of those 3-input AND gates, a "set" state inhibits input J so that the flip-flop acts as if J=0 while K=1 when in fact both are 1. On the next clock pulse, the outputs will switch ("toggle") from set (Q=1 and not-Q=0) to reset (Q=0 and not-Q=1). Conversely, a "reset" state inhibits input K so that the flip-flop acts as if J=1 and K=0 when in fact both are 1. The next clock pulse toggles the circuit again from reset to set.

**PROCEDURE:**

1. Connect the circuit as shown in figure.
2. Apply the 5v on the pin no.5 and GND at pin no.13.
3. Verify the truth table for j-k flip flop with the different connection of input terminal.
4. The SD is use for set and rd is used for reset.

**PRECAUTIONS:**

1. Connect the circuit carefully.
2. Connection should be tight and properly connected.
3. $V_{CC}$ does not exceed more than 5v.
4. Check the LED before use in circuit.

**RESULT**