M. Tech. 1st Semester (EEE)

Examination, December 2024

POWER ELECTRONICS DRIVES CONTROL

Paper : MTEEE-501

Time allowed : 3 hours] *[Maximum marks : 100*

Note: *Attempt **five** questions selecting **one** from each section and **rest one** from any section.*

Section-A

1. (a) Describe the classification of the load torque in drive system.

   (b) Describe the multi-quadrant operation of drive system.

2. Draw and explain the circuit diagram for GTO chopper with snubber-circuit. Also discuss its turnoff characteristics.

Section-B

3. Explain various types of braking for separately excited d.c. motor.

4. Write down the comparative study for armature control in 3-phase motor.

Section-C

5. Explain the principle of operation of step-up and step down chopper.

6. Explain the multiquadrant control of chopper fed motor.

Section-D

7. Write down the current controlled PWM inverter with neat and clean diagram.

8. Explain the four quadrant control and closed loop operation of an induction motor.

23676

M.Tech. 1st Semester (EEE) Examination,

November-2023

POWER ELECTRONICS DRIVES CONTROL

Paper–MTEEE-501

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions in all, selecting **one** question from each section.*

Section–A

1. Explain Multiquadrant operation and speed control of drives. 20

2. Discuss about the circuit symbol and characteristics of Power Transistors and GTO. 20

Section-B

3. Discuss about the operation of three phase half controlled rectifier fed DC motor. 20

4. Explain control rectifier circuits of DC motor. 20

Section–C

5. Explain principle of operation and control techniques of chopper fed DC motor. 20

6. Discuss about the regenerative breaking of chopper fed separately excited and series DC motors. 20

Section–D

7. Explain variable frequency control from voltage sources. 20

8. Explain current controlled PWM inverter and closed-loop control of current controlled PWM inverter fed Induction Motor. 20

Roll No. .....

23676

M. Tech. 1st Semester (EEE) Examination – January, 2023

POWER ELECTRONICS DRIVE CONTROL

Paper : MTEEE-501

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any ***five*** questions. All questions carry equal marks.

1. Explain natural and force commutation of power MOSFET with voltage and current waveform. 20

2. Explain speed control and multiquadrent operation of Power Semiconductor Controlled Drives. 20

3. Draw and Explain the power circuit of a single phase fully controlled rectifier control of a DC separately excited motor. Also draw the waveform at discontinuous mode and speed torque characteristics. 20

4. Derive the equation for critical speed of single phase fully controlled rectifier control of a DC separately excited motor. 20

5. Explain the operation of chopper fed DC drive with both time ratio control and current control. 20

6. A separately excited DC motor is supplied from a DC chopper. Enumerate a relationship between motor parameter, range of motor speed and range of duty cycle. 20

7. (i) What are AC drives ? Give merits and demerits of AC drive with respect to DC drive. 10

   (ii) Enumerate the various methods of speed control of 3-phase motor when fed through semi-conductor device. 10

8. Explain V/F control for 3-phase induction motor for its seep control. Enumerate its advantages. Describe at least two inverter circuits used for V/F control. 20

23677

M.Tech. (EEE) 1st Semester

Examination, December - 2024

ADVANCED MICROPROCESSOR AND CONTROLLER

Paper - MTEEE-503

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt **five** questions in all. **Question No. 1 is compulsory.** Attempt **four** more questions from **sections A, B, C & D** by selecting at least **one** question from each section.*

1. Explain the following : 4×5=20

   (a) Registers

   (b) Interrupts

   (c) Special I/O Devices

   (d) Programming model for 86 family

Section - A

2. Explain Microprocessor Architecture and Memory Addressing Architecture. 20

3. Explain the following : 4×5=20

   (a) Word Length

   (b) Mircroprocessor speed

   (c) Internal Data Bus

   (d) Co-processing

Section - B

4. (a) What do you mean by Interrupt and Polling? What are the Difference between them? 10

   (b) Explain Addressing modes. 10

5. Explain : 2×10=20

   (a) Mnemonics

   (b) DM controllers

Section - C

6. Write short notes on : 2×10=20

   (a) D/A and A/D interface

   (b) UART

7. Draw internal architecture of 8051 and explain each block in details. 20

Section - D

8. Discuss the concept of developing, implementing and testing a design. 20

9. (a) Explain X85 Addressing modes.

   (b) Explain Intel X86 family of Advanced Microprocessor. 2×10=20

M.Tech. 1st Semester (EEE) Examination,

November-2023

ADVANCED MICROPROCESSOR

AND CONTROLLER

Paper–MTEEE-503

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any five questions in all. Each question carries equal marks.*

Section–A

1. Explain the following terms : 2×10=20

(i) Microprocessor's speed characteristics

(ii) Microprocessor Architecture

2. Explain Memory Addressing architecture and the concept of Word Length in Microprocessor. 20

Section-B

3. (i) Discuss in brief about concept of device Polling and Interrupts. 10

(ii) Explain with examples about Addressing Modes in Microprocessor. 10

4. (i) Discuss in detail about instruction set of Microprocessor. Give suitable examples. 10

(ii) Explain Mnemonics in Microprocessor. 10

Section–C

5. Interface DAC 0808 to microprocessor. Draw the interface diagram and addressing mapping. 20

6. (i) Draw and Explain Architecture of 8051. 14

(ii) Discuss in brief about internal RAM of 8051. 6

Section–D

7. For X85 family of microprocessor explain the following :

(i) Addressing Modes 10

(ii) Hardware 10

8. (i) Explain the Design process used to develop a complete Microprocessor based products. 10

(ii) Write short notes on Implementing and Testing a design. 10

Roll No. .....

23677

M. Tech. 1st Semester (EEE) Examination – January, 2023

ADVANCED MICROPROCESSOR AND CONTROLLER

Paper : MTEEE-503

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any *five* questions in all. All questions carry equal marks.

1. Explain the following terms : 20

Speed of Microprocessor, Word Length, Architecture, Parallel Processing

2. (a) Why the lower order address bus is multiplexed with data bus ? How they will be de-multiplexed ? 10

(b) Draw the block diagram of microprocessor and explain. 10

3. (a) Describe the instruction format and addressing modes of microprocessor. 10

(b) Write in detail about device polling and interrupt. 10

4. (a) Explain the DMA method of data transfer in microprocessors. 10

(b) Draw a typical connection diagram to connect I/O devices with microprocessor. Explain the data flow in this. 10

5. Write notes on : 20

(i) Addressing modes in 8051 Microcontroller

(ii) Operation of Timers in 8051

6. (a) Draw a typical connection diagram of D/A interface with microprocessor and explain its working. 10

(b) Explain the operation of UART modems. How it is different from USART ? 10

7. (a) State differences between 8085 and 8086 Microprocessors. 10

(b) Write the data transfer instructions of 8085 Microprocessor and explain taking examples. 10

8. Write notes on :

(a) Design process of a Microprocessor 10

(b) Programming model for 8086 10

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M.Tech. (EEE) 1st Semester

Examination, December-2024

ADVANCED DIGITAL SIGNAL PROCESSING

Paper : MTEEE-505

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempts any **five** questions. All questions carry equal marks.*

1. (a) What is a Digital Processing system? Enlist advantages and disadvantages of digital signal processing over analog signal processing. 10

   (b) Explain Casuality and Stability of linear time Invariant system. 10

2. (a) State the following properties of Fourier Transform : 10

   (i) Duality

   (ii) Convolution

   (b) Explain the process of reconstruction of signal from its samples. Also explain the nyquist rate and problem associated if it is not followed. 10

3. Explain in detail various window functions for the design of FIR filter. 20

4. Perform the circular convolution of two given sequences : 20

$x(n) = [2, 2, 1, 1], h(n) = [4, 3, 2, 1]$

5. (a) Discuss the effects of finite word length in digital filters. Analyse truncation and round off process in binary number representations. 10

(b) Explain the effects of finite precision arithmetic on digital filters. 10

6. Draw the structures of Direct form-1, Direct form-2, Cascade and parallel realization of : 20

$$H(z) = \frac{\frac{z}{6} + \frac{5}{24} + \frac{5}{24}z^{-1} + \frac{1}{24}z^{-2}}{1 - \frac{1}{2}z^{-1} + \frac{1}{4}z^{-2}}$$

7. (a) Find the z-transform : 10

$$x(n) = \begin{cases} 2^n, & for \quad n < 0 \\ (1/2)^n, & for \quad n = 0, 2, 4, 6 \ldots \\ (1/3)^n, & for \quad n = 1, 3, 5, 7 \ldots \end{cases}$$

(b) Give properties of DFT. 10

8. Write notes on : 20

(a) Computation of Fourier and Time sequences from spectra.

(b) Fast Fourier transform.

M.Tech. 1st Semester (EEE)

Examination, November-2023

ADVANCED DIGITAL SIGNAL PROCESSING

Paper - MTEEE-505

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt five questions in all.* ***Question No. 1 compulsory.*** *Attempt four more question from the Sections A, B, C & D by selecting one question from each section.*

1. (a) Define multi rate signal processing and explain any two applications of it.

(b) Write a short note on realization form of IIR filter?

(c) What are the desirable characteristics of the frequency response of window function?

(d) Compare various windows used in the design of FIR filter. 4×5=20

Section-A

2. (a) Check whether the following system is linear and time invariant $F[x(n)] = a[x(n)]^2 + bx(n)$. 10

(b) Explain the following terms w.r.t. DSP

(i) Stability & causality Criterion

(ii) Unit sample response 2×5=10

or

3. (a) State and prove convolution theorem of Fourier transform. 10

(b) State the sampling theorem. For any signal how the sampling rate is selected? Also discuss that if sampling is performed at minimum sampling rate then how reconstruction is done? 10

Section-B

4. Determine circular convolution as well as linear convolution for the sequence

$x_1(n) = \{2, \underset{\uparrow}{1}, 2, 1\}$

and $x_2(n) = \{1, \underset{\uparrow}{2}, 3, 4, 5\}$ 20

or

5. Explain in detail various window functions for FIR filter. 20

Section-C

6. (a) Draw the structure of cascade and parallel realization of

$$H(z) = \frac{(1-z^{-1})}{(1-.5z^{-1})(1-.125z^{-1})}$$ 10

(b) Discuss the effects of finite precision arithmetic on Digital filters. 10

or

7. (a) Discuss the direct form of cascaded realization of (IIR) filter. 10

(b) Discuss different designing techniques of digital filter. 10

Section-D

8. (a) State and prove convolution and correlation properties of Z-transform. 10

(b) Using long division, determine the Z-transform of

$$X(z) = \frac{1+2z^{-1}}{1-2z^{-1}+z^{-2}}$$ 10

or

9. Compute the 16 point DFT of sequence

$x(n) = \cos(\pi/2)n$ using radix-4 DITFFT. 20

Roll No. .....

23678

M. Tech. 1st Semester (EEE) Examination – January, 2023

ADVANCED DIGITAL SIGNAL PROCESSING

Paper : MTEEE-505

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all, selecting *one* question from each Section. Question No. 1 is *compulsory*. All questions carry equal marks.

1. (a) Explain stability and causality of a signal.

$4 \times 5 = 20$

(b) List out the differences between linear convolution and circular convolution.

P. T. O.

(c) How FFT is more efficient to determine DFT of sequence ?

(d) Write a short note on realization form of FIR filter.

SECTION – A

2. (a) Explain all types of system with suitable examples. 10

(b) Classify Discrete Linear Systems ? Explain its properties in detail. 10

3. (a) Find the Fourier transform of : 10

$$x(n) = a^n \cos w_0 n\, u(n)$$

(b) What are the basic elements of digital Signal Processing ? List the advantages of digital signal processing over analog signal processing. 10

SECTION – B

4. Explain in detail various window functions for FIR filter Design. 20

5. Write short notes on : $10 \times 2 = 20$

(a) Phase Equalizer

(b) Digital Frequency Transformation

SECTION – C

6. (a) Discuss the effect of finite word length in digital fitter. 10

(b) Obtain a cascade and parallel realization of the system characterized by the transform function 10

$$H(z) = \frac{2(z+2)}{z(z-0.1)(z+0.5)(z+0.4)}$$

7. (a) Discuss the different design techniques of digital filter. 10

(b) Discuss the parallel realization of IIR filter. 10

SECTION – D

8. (a) Explain the properties of DFT. 10

(b) Determine the z-transform and ROC of signal 10

$$x(n) = [3(2^n) - 4(3^n)]\, u(n)$$

9. (a) Discuss various properties of DFT. 10

(b) What is the need of FFT algorithm ? State its computational requirements. 10

M. Tech. 1st Semester (EEE)

Examination, December 2024

ADVANCED COMPUTER POWER SYSTEM ANALYSIS

Paper : MTEEE-507

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt* ***five*** *questions in all, selecting* ***one*** *question from each unit.*

Unit–1

1. Explain the dynamic programming approach in unit commitment. 20

2. Write short note on : 20

   a. Ferranti

   b. State estimation

Unit–2

3. Explain the Gauss-Seidel method for load flow study. 20

4. Explain the N-R method for load flow study. 20

Unit–3

5. Explain the load frequency control in two area control with its overall transfer function. 20

6. Write short note on : 20

   a. Tie-time bias control

   b. Essential need of frequency constant.

Unit–4

7. A 05 MVA 11 kV alternator with solidly grounded neutral has a sub transient reactance of 0.5 pu. The negative and zero sequence reactances are 0.3and 0.5 pu respectively. A single line to ground fault occurred at the terminal of unloaded alternator. Determine the fault current and line to line voltage. 20

8. Define the expression of fault current for double line to ground fault. 20

M.Tech. 1st Semester (EE)

Examination, November-2023

ADVANCED COMPUTER POWER SYSTEM ANALYSIS

Paper - MTEEE-507

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Each question carries equal mark (20 marks). Students have to attempt 5 questions in total.*

1. (a) Explain with a neat flowchart the procedure for finding the solution for unit commitment Problems using forward DP method. 20

2. (a) There are three thermal generating units which can be committed to take the system load. The fuel cost data and generation operating unit data are given below :

$F1 = 392.7 + 5.544\ P\ 1 + 0.001093\ P\ 12$

$F2 = 217 + 5.495\ P\ 2 + 0.001358\ P\ 22$

$F3 = 65.5 + 6.695\ P\ 3 + 0.004049\ P$

P 1, P 2, P 3, in MW Generation limits :

$150 \leq P\ 1 \leq 600$ MW ; $100 \leq P\ 2 \leq 400$; $50 \leq P\ 3 \leq 200$ MW. There are no other constraints on system operation. Obtain an optimum unit commitment table. Adopt Brute force enumeration technique. Show the details of economic schedule and the total costs of operation for each feasible combination of units for the load level of 900. 20

3. The load flow data for the sample power system are given below. The voltage magnitude at bus 2 is to be maintained at 1.04 p.u. the max and min reactive power limits of the generator at bus 2 are 0.35 and 0.0 p.u. respectively. Determine the set of load flow equation at the end of first iteration by using G-S method: 20

Bus code	Impedance	Line charging admittance
1-2	0.06+j0.30	0
1-3	0.04+j0.12	0
2-3	0.08+j0.22	0

Schedule of generation of loads:

Bus code	Assumed voltage	Generation		Load	
		MW	MVAR	MW	MVAR
1	1.06+j0.0	0	0	0	0
2	1.00+j0.0	0.2	0	0	0
3	1.06+j0.0	0	0	0.6	0.25

4. Derive N-R method of load flow algorithm and explain the implementation of this algorithm with the flowchart. 20

5. Discuss in detail the dynamic response of a single area system, without integral control, following a step load disturbance. 20

6. Draw the tranfer function block diagram for a two area system provided with governor control and obtain the steady state frequency error following a step load change in both the areas. 20

7. (a) Draw the +ve, -ve and zero sequence networks of synchronous machine. 10

   (b) Sketch the zero sequence equivalent circuits of a transformer. 10

8. Explain the step by step procedure to find the fault current of three phase symmetrical fault by using Thevenin's theorem. 20

Roll No. .....

23679

M. Tech. 1st Semester (EEE) Examination – January, 2023

ADVANCED COMPUTER POWER SYSTEM ANALYSIS

Paper : MTEEE-507

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all. All questions carry equal marks.

1. Explain with a neat flowchart the procedure for finding the solution for unit commitment Problems using backward DP method. 20

2. (a) Deduce an expression for voltage regulation of a short transmission line, giving the vector diagram. 10

(b) Write short note on Priority list scheme method. 10

3. Determine the voltages at all the buses at the end of first iteration using GS method. 20

Line data :

Bus Code	Admittance (p.u.)
1-2	1 + j6
1-3	2 – j3
2-3	0.8 – j 2.2
2-4	1.2 – j 2.3
3-4	2.1 – j 4.2

Load data :

Bus No.	P (p. u.)	Q (p. u.)	V (p. u.)	Remarks
1	–	–	1.03	Slack
2	0.52	0.23	1.0	PQ
3	0.42	0.32	1.0	PQ
4	0.4	0.12	1.0	PQ

4. Derive N-R method of load flow algorithm and explain the implementation of this algorithm with the flowchart. 20

5. Draw the block diagram of load frequency control for single area. And explain it. 20

6. Draw the transfer function block diagram for a two area system provided with governor control and obtain the steady state frequency error following a step load change in both the areas. 20

7. A 25 MVA, 13.2 KV alternator with solidly grounded neutral has a sub transient reactance is 0.25 the negative and zero sequence reactance are 0.35 and 0.01 p.u. respectively if a double line to ground fault occurs at the terminals of the alternator. Point out the fault current and line to line voltage at the fault. 20

8. (a) What are symmetrical components ? Explain the utility of symmetrical components in short circuit analysis. 10

(b) Derive an expression for power in a 3-phase circuit in terms of symmetrical components. 10

M. Tech. 1st Semester (EEE)
Examination, December–2024
COMPUER CONTROL SYSTEM
Paper-MTEEE-513

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt **five** questions by selecting **one** questions from each unit.*

Unit-I

1. (i) Explain the distributed versus centralized digital control system. 10

   (ii) Explain the advantages of digital control system. 10

2. Write short note on : 20

   (i) Fibre optics transducer

   (ii) System architecture of digital control system

Unit-II

3. Write short note on : 20

   (i) Interrupt system

   (ii) Input-output software

4. Write short note on : 20

   (i) LAN

   (ii) Serial interface

Unit-III

5. Explain real time operating system. 20

6. Write short note on : 20

   (i) Inter task communication

   (ii) Task management

Unit-IV

7. Explain the illustration of PLC and SCADA in petrochemical plant. 20

8. Explain the application of PLC to process the control SCADA system. 20

23680

M.Tech. 1st Semester (EEE) Examination,

November-2023

COMPUTER CONTROL SYSTEM

Paper–MTEEE-513

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions in all, selecting **one** question from each unit. Each question carries equal marks.*

Unit–I

1. Explain analogue to digital and digital to analogue convert. 20

2. Write short note on : 20
   (i) Intelligent sensor
   (ii) Silicon transducers

Unit-II

3. Explain serial communication line and parallel database in detail. 20

4. Write short note on : 20
   (i) IEEE 4888
   (ii) WAN

Unit–III

5. Explain real time operating system versus real time programming language. 20

6. Write short note on : 20

   (i) Multitasking

   (ii) Task Management

Unit-IV

7. Explain the illustration of PLC and SCADA in power plant. 20

8. Explain the principle of operation and architecture of PLC. 20

Roll No. .....

23680

M. Tech. 1st Semester (EEE) Examination – January, 2023

COMPUTER CONTROL SYSTEM

Paper : MTEEE-513

Time : Three Hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

UNIT – I

1. (i) What are the advantages of digital control system ? 20

   (ii) Explain digital/analog converters.

P. T. O.

2. Write short notes on : 20

(i) Fibre optic transducer.

(ii) Bio-transducer.

UNIT – II

3. Explain the various input/output software in computer network. 20

4. Explain serial communication lines and parallel database in computer network. 20

UNIT – III

5. Explain real time operating system versus real time programming language. 20

6. Write short notes on : 20

(i) Intertask communication.

(ii) Multitasking.

UNIT – IV

7. Explain the application of PLC and SCADA in power plant. 20

8. Write short notes on : 20

(i) Software configuration of PLC.

(ii) Architecture of PLC.
